Effects of Buffer Layer and thickness of window-layer on performance of Highly Efficient Polycrystalline Cadmium Sulfide (CdS)/Cadmium Telluride (CdTe) Solar cells

M Thanihaichelvan[1], P. Ravirajan[1]*, GDK Mahanama[2], MAKL. Dissanayake[3], E. Colegrove[4,5], R. Dhere[4,5]and S. Sivananthan[4,5]

(1)Department of Physics, University of Jaffna, Thirunelveli, JA 40 000, SRI LANKA
(2)Department of Physics, University of Ruhunu, Matara, SRI LANKA
(3)Institute of Fundamental Studies, Kandy, SRI LANKA
(4) Department of Physics, University of Illinois at Chicago, Chicago, USA
(5)Sivananthan Laboratories Inc., Bolingbrook, USA
* pravirajan@gmail.com

Abstract

In this work, the effects of buffer layer and thicknesses of the window layer on performance of CdS/CdTe solar cells were studied. The quality and performance of the buffer layer and active layers was studied as a function of CdS layer thickness using atomic force microscopy and current density – voltage measurements of the corresponding cells, respectively. Short-circuit current density is significantly enhanced by introducing a buffer layer between bottom electrode and CdS. It is also highly dependent on the thicknesses of the window layer and is optimized for a window layer thickness of 50 nm. The optimized devices showed external quantum efficiencies over 85 % at the maximum absorption wavelengths of cadmium telluride and yield short circuit current densities up to 24 mAcm^{-2} for air mass (AM) 1.5 conditions (100 mW cm^{-2}, 1 sun). The AM 1.5 open circuit voltage reaches 0.82 V and the fill factor 0.73, resulting in an overall power conversion efficiency over 14 %.

1. Introduction

CdTe is one of the most popular material for solar-electrical energy conversions as the record efficiencies reached 18.7 % at 2013. But, it is long way to go to reach the theoretical maximum efficiency around 29.5 %. The important loss in superstrate design is the absorption of CdS window layer. Thin layers report relatively high J_{SC} but low V_{OC}. It is reported that the pinholes in the thin CdS causes the fall in V_{OC}. The Roughness of the TCO film also may affect the presence of pinholes.

2. Experimental

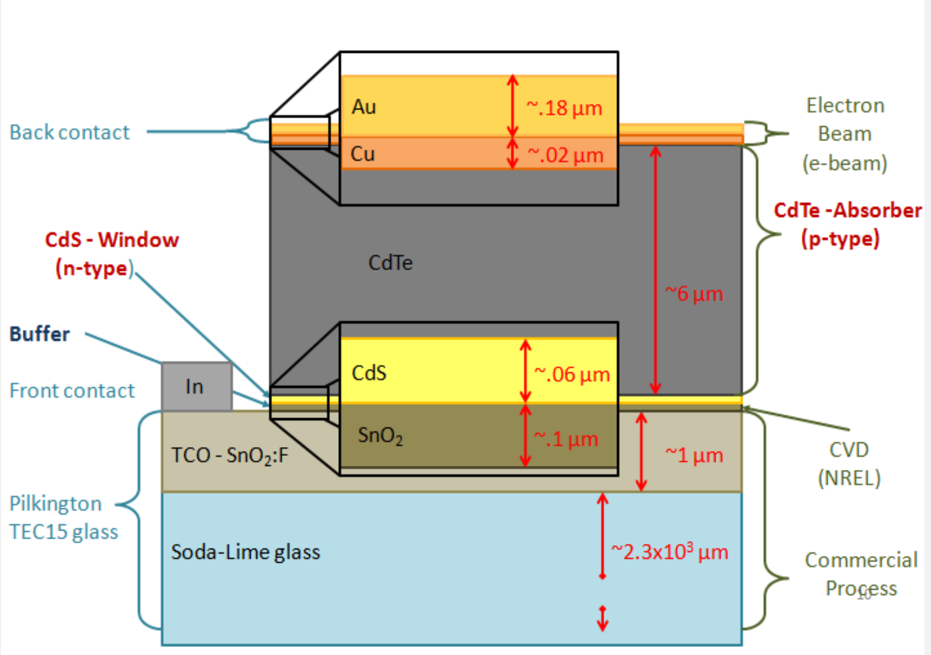

Fig 1. Optimized cell structure.

- ❖CdS layer grown by Chemical bath deposition.
  - ▪ Thickness variation obtained by changing the deposition time.
- ❖CdTe layer by Close Space Sublimation.
- ❖SnO_2 buffer layer by Chemical vapor deposition.
- ❖Top contacts by Electron beam deposition.
- ❖Four types of devices have made .
  - [1] Thin (50 nm) CdS without buffer layer.
  - [2] Thin (50 nm) CdS with buffer layer.
  - [3] Thick (80 nm) CdS without buffer layer.
  - [4] Thick (80 nm) CdS with buffer layer.
- ❖ CdTe layer kept constant for all four devices.

3.2 External Quantum efficiency measurements

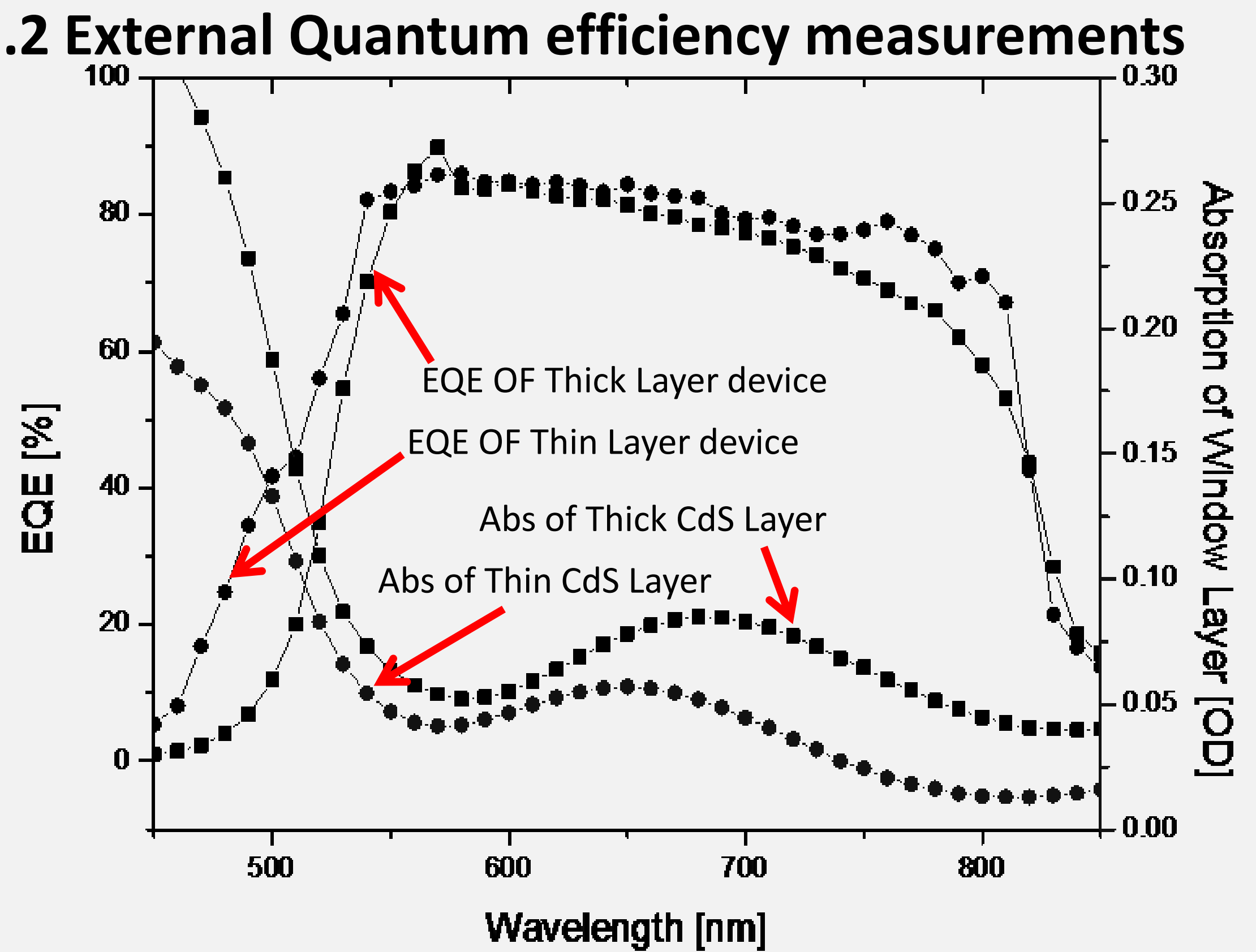

Fig 3. The EQE spectra of the CdS/CdTe solar cells with thick and thin window layers with the absorption spectra of the thick and thin CdS films.

- ❖ The Quantum efficiency spectra clearly shows the variation in the region below 550 nm due to the absorption of CdS window layer.
- ❖ The scattering in the red region also considerably high for the thick CdS layer.
- ❖ The thin CdS is more transparent which enhances the spectral use of the cell.
- ❖ The slope in deep penetration at 850 nm is due to the scattering.

3. Results

3.1 Comparison of cell performance, J-V Measurements

Short Circuit Current Density (J_{SC}) | **Open circuit Voltage (V_{OC})** | **Fill factor (%)** | **Power Conversion efficiency (%)**

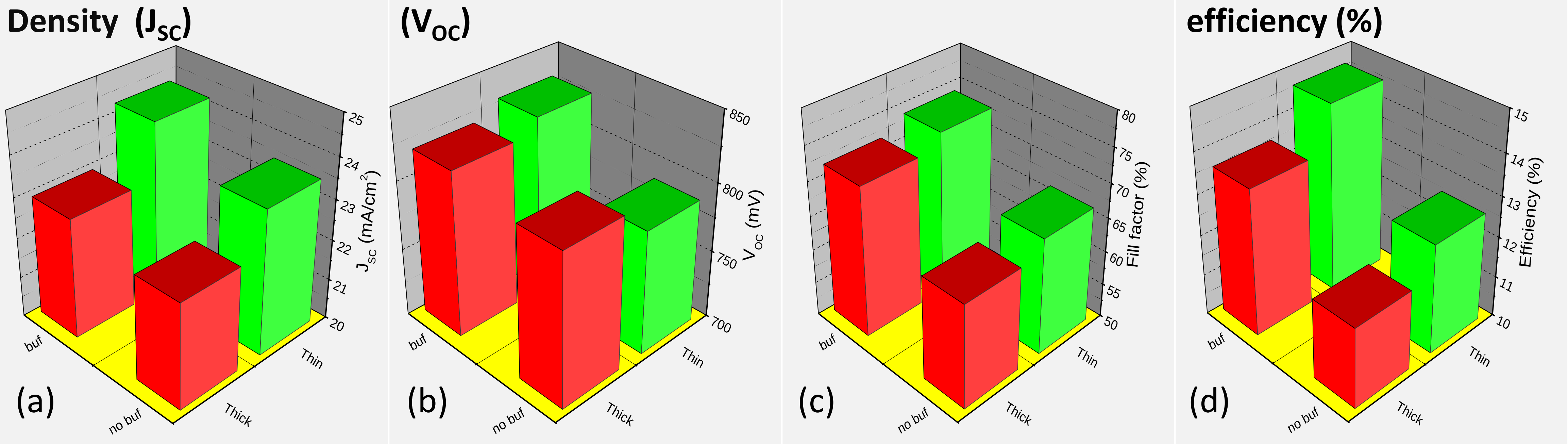

Fig 2. Comparison of (a) JSC, (b) VOC, (c) Fill factor and (d) Conversion efficiencies of the fabricated thin and thick CdS layer devices with and without buffer layer.

Short Circuit Current Density (J_{SC})	Open circuit Voltage (V_{OC})	Fill factor (%)	Power Conversion efficiency (%)
❖J_{SC} of the thin CdS device is more than that of thick CdS device. ❖J_{SC} of the thin CdS device increases rapidly with presence of buffer layer. ❖No significant changes in thick CdS layer device due to the buffer layer.	❖ V_{OC} of the thick CdS layer device is grater than that of thin layer device. ❖ V_{OC} of the thin CdS layer device improved nearly equal to that of the thick film device when the buffer layer is introduces.	❖ Fill factor is strongly depends on the buffer layer. ❖ The fill factor has improved nearly 8 % after the buffer layer is introduced.	❖ Presence of buffer layer improves the conversion efficiencies considerably. ❖ With buffer layer, the thin film device shows maximum conversion efficiency.

3.3 Roughness of buffered and unbuffered surfaces

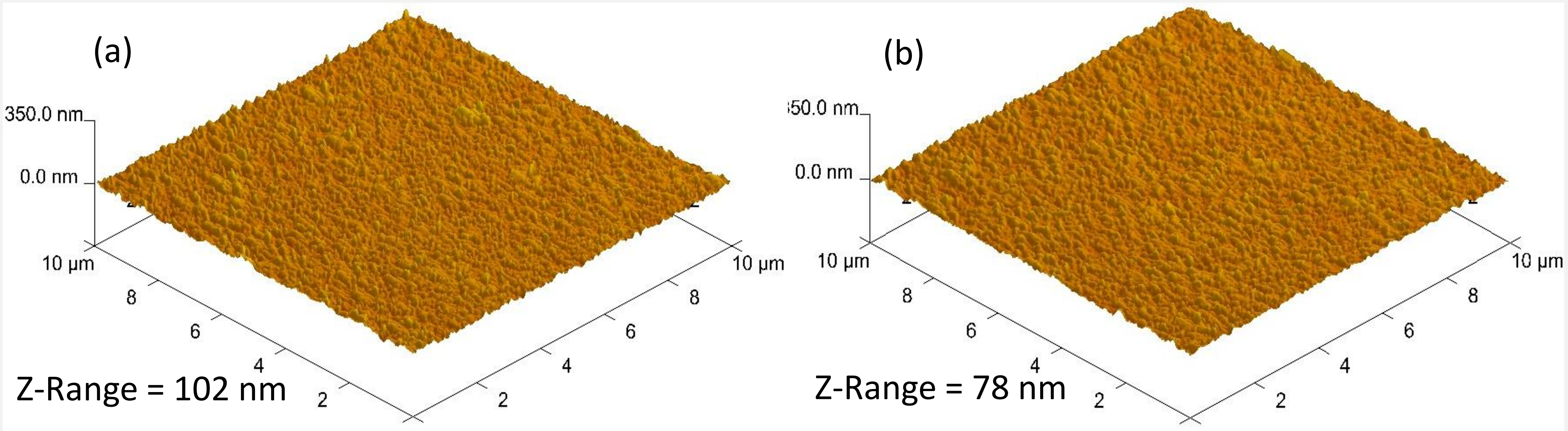

Fig 4. The AFM image of (a) bare FTO used for cell fabrication and (b) FTO/Sputtered SnO_2 buffer layer glasses.

- ❖ The Z ranges of the surfaces were 78 nm and 102 nm respectively.
- ❖ The Z-Range of the unbuffered TCO layer is nearly double of the thickness of thin CdS layer.
- ❖ Sharp pin shaped nanostructures also observed in the unbuffered ITO layer.
- ❖ This may increases the probability of presence of pinholes and formation localized TCO/CdTe contacts during the high temperature deposition of CdTe layer which reduce the V_{OC} .
- ❖ The presence of buffer layer smooth the TCO surface and provide a barrier layer to avoid TCO/CdTe contacts that results drop in V_{OC}.

4. Conclusions

- ❖ Thin CdS layer with improved transmission makes the J_{SC} better.
- ❖ Buffer layer smoothes the surface and reduce the presence of pin holes in CdS layer.
- ❖ The buffer layer avoids the TCO – CdTe junctions and improves the fill factor and V_{OC} for the thin CdS layer device.
- ❖ High efficiency of nearly 15 % is achieved for an optimized CdS/CdTe device with thin CdS and buffer layer.

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